



Sheet 1 of 1

FORM PTO-1449
(REV.7-80)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT
(Use several sheets if necessary)

ATTY. DOCKET NO.
851663.422USPC

APPLICATION NO.
09/807,500

APPLICANTS
Rakesh Malik and Puneet Goel

FILING DATE
June 11, 2001

GROUP ART UNIT
2171 2124

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AA						
AB						<i>RECEIVED</i>
AC						<i>JAN 18 2002</i>
AD						<i>Technology Center 2100</i>
AE						
AF						
AG						
AH						
AI						
AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION
					YES NO
CD	AK	WO 94/23493	10/13/94	WIPO	
	AL				
	AM				
	AN				

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

CD	AO	Dawood Alam et al, "VLSI Implementation of a New Bit-Level Pipelined Architecture for 2-D Allpass Digital Filters," <i>Institute of Electrical and Electronics Engineers</i> , 1: 724-727, April 30-May 3, 1995.
CD	AP	K. Manivannan et al., "Minimal Multiplier Realization of 2-D All-Pass Digital Filters", <i>IEEE Transactions on Circuits and Systems</i> , 35(4):480-484, April 1998.
CD	AQ	Rakesh Malik and Puneet Goel, "Area-Minimal-Architecture-in-Bit-serial-FIR-Filters", <i>Proceedings of the European Conference on Circuit Theory and Design ECCTD'99</i> , Stresa, Italy, August 29-September 2, 1999, p. 719-722.

EXAMINER

DATE CONSIDERED

2/10/04

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).